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CONDUCTOR LINE STRUCTURE AND METHOD FOR IMPROVED BORDERLESS CONTACT PROCESS TOLERANCE

Abstract

A structure and method are provided for a conductor line stack of an integrated circuit. The conductor line stack includes a layer of a first material such as heavily doped polysilicon or a metal silicide. A layer of a second material such as a metal is formed over the layer of first material, the layer of second material having an upper portion and a lower portion. A pair of first spacers is disposed on sidewalls of the upper portion, wherein the lower portion has width defined by a combined width of the upper portion and the pair of first spacers. A pair of second spacers is formed on sidewalls of the first spacers, the lower portion and the layer of first material. The conductor line stack structure is well adapted for formation of a borderless bitline contact in contact therewith.